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METROLOGY IS KEY TO COST CONTROL IN THE SEMICONDUCTOR INDUSTRY

BY GAIL B. STOUT

☐ What drives the semiconductor industry? What new whiz-bang will keep the US on top in the high-tech innovative area of electronics? The semiconductor industry today has become practical, along with the rest of the manufacturing world, and is focusing on cost control.

Electronic tools—the end products of past innovation in chip technology—are being used in simulation computer-integrated manufacturing (CIM) equipment. And metrology is the key to improving the cost of owning a fab (wafer fabrication plant) when comparing its optimum performance (a virtual simulated fab model) with its actual efficiency level.

Because metrology has a finger on a fab's pulse, it plays an increasingly vital role in manufacturing, according to attendees at a recent Semiconductor Equipment and Materials International (SEMI) North American Regional Standards Planning Meeting in Chandler, AZ. The standards group set industry goals through the year 2007. SEMI members attending the standards meeting came from IBM, National Semiconductor, AT&T Microelectronics, NCR Corp., Intel, AMD, the National Institute of Standards and Technology (NIST), Texas Instruments, and 11 volunteers from Semiconductor Manufacturing Technology (SEMATECH—a consortium of government, semiconductor manufacturers, and academe). As part of an intense, four-day planning process, every standard was reviewed to ensure its future applicability.

Because the cost of owning a fab has become critical to survival for US semiconductor companies, controlling costs is vital to US competitiveness. The cost of building a production facility, or fab, is over $1 billion. To keep costs in line, wafer manufacturers and suppliers are working to lower the cost of purchasing and running semiconductor equipment.

Cost control starts with projecting what costs will be under "what if" circumstances. SEMI is writing software to evaluate fab designs, process recipes, material substitutions, and flexible manufacturing alternatives before breaking ground on a fab. For an existing plant, software modeling will provide optimum performance data to CIM controls.

Then the complexity begins. Standards required to link the predicted "virtual" fab to the actual fab are difficult. And standards must be created to model each detail that goes into the cost of building a fab: equipment, processes, materials, and the facility. A common language must allow linkage from virtual fab to library data on optimum performance characteristics with real data from fab's CIM system. Semiconductor manufacturers are building the common language standard and plan to meet this challenge by the year 2000.

Three stages of IC production in a fab. From left to right, lapping and polishing silicon wafers to a mirrorlike finish is an early stage. Wafers are diced into chips with a diamond-bladed saw. Individual chips are mounted into lead frames.

How does measurement enter into this process? As new materials for wafer fabrication are introduced and as smaller geometries for advanced circuits are used, standards must be developed to deal with their use within the virtual fab model. One problem along this line is wafer size.

Wafers with a 200 mm diameter are the norm. Although there already is a 300 mm wafer standard in the SEMI standards book, what should be the next wafer size—400 mm? Should the wafer shape remain a circle or would a rectangular substrate shape be more manufacturable and less costly? These issues are under consideration by the standards committee.

Metrology is the key to unlock the uncertainty of a fab's optimum performance. Metrology standards cross many disciplines to evaluate materials and equipment performance and interaction. Current metrology standards concentrate on gas distribution, liquid chemical distribution, and purity specifications. Ongoing standards work focuses on test guidelines in these areas:

- Thermal conductivity test methods.
- Multichip module test chips.
- Multichip module tests for incoming materials.
- Alpha particle emission tests.

Roadmaps are under development to link these test guidelines and standards efforts to the cost of ownership of computer-simulated models for justification of equipment performance criteria.

Multichip modules (MCMs) are recent semiconductor innovations. Because they are so new, standards for test have not been fully established. MCMs are made from bare dice connected in one complex layered-module. They are predicted to be the next electronics building blocks to systems requiring speeds of more than 50 mHz. Rather than the usual practice of mounting a single chip into an individual package and then connecting the leads to a board, with MCMs many chips are interconnected directly in one module. The density and complexity of an MCM is greatly increased over today's board-testing methods. And with reduced size, yet increased density, building and testing standards are critical.

According to John Schuler, manager of quality and organizational systems at SEMI, "Metrology, including test, measurement, documentation, and control, are important to US competitive strategies. In situ, on-line automated metrology is the key to the future. Our manufacturing equipment must be smart enough to self-correct." ☐

GAIL B. STOUT is a senior editor of Quality.

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